

by: NXP Semiconductors

1 Introduction

Sometimes, user would like to keep the MCU's application software (firmware) on the external memory media, so that various kinds of way of downloading the firmware can be supported. This feature is also useful for the engineers to demonstrate various examples project with only one hardware board. When the program cannot be downloaded to the chip directly in some reason (for example, the additional license requirements or the additional equipment requirements), switching the memory media with different firmware is more acceptable.

This application note describes a design of 2nd bootloader, using SD card as the external memory media to keep the firmware image files to be executed. The example projects, including the bootloader project and firmware project, are developed originally on the LPCXpresso54608 EVK board. The SD card is chosen as the external memory, as it sets up a file system where the PC can directly read and write the files.

After the POR, the bootloader software in the chip's internal flash runs first. It reads the SD card to detect the available firmware image files and tells the available options to users through the terminal, based on the UART. Users make the selection, and then the bootloader software loads the selected image files from SD card to the chip's internal memory, SRAM, and execute.

2 Hardware

2.1 LPC54608 MCU

The LPC54600 is a family of Arm® Cortex®-M4 based microcontrollers for embedded applications featuring a rich peripheral set with very low power consumption and enhanced debug features.

The LPC54600 family includes up to 512 KB of flash, 200 KB of on-chip SRAM, up to 16 KB of EEPROM memory, a quad SPI Flash Interface (SPIFI) for expanding program memory, one high-speed and one full-speed USB host and device controller, Ethernet AVB, LCD controller, Smart Card Interfaces, SD/MMC, CAN FD, an External Memory Controller (EMC), a DMIC subsystem with PDM microphone interface and I²S, five general-purpose timers, SCTimer/PWM, RTC/alarm timer, Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), ten flexible serial communication peripherals (USART, SPI, I²S, I²C interface), Secure Hash Algorithm (SHA), 12-bit 5.0 M samples/sec ADC, and a temperature sensor.

Contents

1	Introduction.....	1
2	Hardware.....	1
2.1	LPC54608 MCU.....	1
2.2	LPCXpresso54608 EVK board....	2
3	Software.....	3
3.1	Edit the linker files to re-allocate the memory space.....	3
3.2	Jump to execute the new image..	5
3.3	Use the cJSON middleware to read configuration file on SD card.....	5
4	Run demo project.....	6



Type number	Package Name	Frequency/MHz	Flash/kB	SRAM/kB	FS USB	HS USB	Ethernet AVB	Classic CAN	CAN FD	LCD	Flexcomm Interface	EMC data bus width (bit)	GPIO	SHA
LPC54628 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0, LCD, SHA)														
LPC54628J512ET180	TFBGA180	220	512	200	yes	yes	yes	yes	yes	yes	10	8/16	145	yes
LPC54618 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0, LCD)														
LPC54618J512ET180	TFBGA180	180	512	200	yes	yes	yes	yes	yes	yes	10	8/16	145	no
LPC54618J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	yes	yes	10	8/16/32	171	no
LPC54616 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0)														
LPC54616J256ET180	TFBGA180	180	256	136	yes	yes	yes	yes	yes	no	10	8/16	145	no
LPC54616J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	yes	no	10	8/16/32	171	no
LPC54616J512ET100	TFBGA100	180	512	200	yes	yes	yes	yes	yes	no	9	8/16	64	no
LPC54616J512BD100	LQFP100	180	512	200	yes	yes	yes	yes	yes	no	9	8/16	64	no
LPC54608 devices (HS/FS USB, Ethernet, CAN 2.0, LCD)														
LPC54608J512ET180	TFBGA180	180	512	200	yes	yes	yes	yes	no	yes	10	8/16	145	no
LPC54608J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	no	yes	10	8/16/32	171	no
LPC54607 devices (HS/FS USB, LCD)														

Figure 1. LPC54608 MCU in the LPC54600 family

In this application example, the LPC54608J512ET180 part is used.

Figure 2 shows the location of the internal memory.

Address range	General Use	Address range details and description	
0x0000 0000 to 0x1FFF FFFF	On-chip non-volatile memory	0x0000 0000 - 0x0007 FFFF	Flash memory (512 kB).
	Boot ROM	0x0300 0000 - 0x0300 FFFF	Boot ROM with flash services in a 64 kB space.
	SRAMX	0x0400 0000 - 0x0400 7FFF	I&D SRAM bank (32 kB).
	SPI Flash Interface (SPIFI)	0x1000 0000 - 0x17FF FFFF	SPIFI memory mapped access space (128 MB).
0x2000 0000 to 0x3FFF FFFF	SRAM Banks	0x2000 0000 - 0x2002 7FFF	SRAM banks (160 kB).
	SRAM bit band alias addressing	0x2200 0000 - 0x23FF FFFF	SRAM bit band alias addressing (32 MB)

Figure 2. LPC54608 internal memory for FLASH and SRAM (with SRAMX)

2.2 LPCXpresso54608 EVK board

The example projects, including the bootloader project and application projects, are developed originally on the LPCXpresso54608 EVK board. Actually, for the bootloader feature, the minimal requirement of hardware board is just with an SD card socket, as shown in Figure 3.

Generally, the bootloader's code is placed in the on-chip FLASH, and the data is placed in a piece of standalone internal SRAM (SRAMX, 32 KB, starting from 0x0400_0000). The firmware's code and data are all placed in the continuous memory space starting from 0x20000000, as shown in [Table 1](#).

Table 1. Allocation of the memory space for bootloader and firmware project

Function	Address	Size
Bootloader code	0x0000_0000 - 0x0007FFFF	512 KB
Bootloader data	0x0400_0000 - 0x04007FFF	32 KB
Firmware code	0x2000_0000 - 0x2001FFFF	128 KB
Firmware data	0x2002_0000 - 0x20027FFF	32 KB

Actually, these settings take effect in the linker files for each project. In the current example, there are two linker files:

1. Bootloader project's linker file

```
define symbol m_interrupts_start      = 0x00000000;
define symbol m_interrupts_end       = 0x000003FF;

define symbol m_text_start           = 0x00000400;
define symbol m_text_end             = 0x0007FFFF;

define symbol m_data_start           = 0x04000000;
define symbol m_data_end             = 0x04007FFF;

...
```

2. Firmware project's linker file

```
define symbol m_interrupts_start      = 0x20000000;
define symbol m_interrupts_end       = 0x200003FF;

define symbol m_text_start           = 0x20000400;
define symbol m_text_end             = 0x2001FFFF;

define symbol m_data_start           = 0x20020000;
define symbol m_data_end             = 0x20027FFF;

...
```

In both linker files, I enlarged the size of stack and heap for the default settings to provide enough resource for the following usage of cJSON. In the example projects, the stack size and the heap size are all with 4 KB.

```
/* Sizes */
if (isdefinedsymbol(__stack_size__)) {
    define symbol __size_cstack__      = __stack_size__;
} else {
    define symbol __size_cstack__      = 0x1000;
}

if (isdefinedsymbol(__heap_size__)) {
    define symbol __size_heap__        = __heap_size__;
} else {
```

```

define symbol __size_heap__ = 0x1000;
}

```

Actually, since the memory space is totally independent, the firmware project can be downloaded and debugged (into SRAM) directly without the regarding of bootloader. It can run normally under the control of the debugger.

3.2 Jump to execute the new image

To jump to execute the new image, manually fill the SPs (MSP and PSP) and the PC registers with the address for the new image. In this example, I used the traditional piece of code as following:

```

/* execute the firmware exists in sramx. */
typedef void(*func_0_t)(void);
void app_execute_ram_firmware(void * addr)
{
    uint32_t * vector_table = (uint32_t *)addr;
    uint32_t sp_base = vector_table[0];
    func_0_t pc_func = (func_0_t)(vector_table[1]);

    /* set new msp and psp. */
    __set_MSP(sp_base);
    __set_PSP(sp_base);
#ifdef __VTOR_PRESENT == 1
    SCB->VTOR = addr;
#endif
    /* jump to application. */
    pc_func();
    /* the code should never reach here. */
    while (1)
    {}
}

```

3.3 Use the cJSON middleware to read configuration file on SD card

cJSON is an open source middleware component of parsing the JSON text existing in [GitHub - DaveGamble/cJSON: Ultralightweight JSON parser in ANSI C](#). It is coded with pure C to be integrated into any embedded system without any porting work related to the platform.

In this example, cJSON was used to parse the configuration file written in JSON format, which is a popular way used in Python programming. The *conf.json* file was placed in the SD card with the image files. It recorded the information about all the available image files. Then the bootloader read to find the real image file according to the configuration file. The content of the *conf.json* file was as below:

```

{
    "default":
    {
        "idx":1,
        "num":2
    },
    "filepaths":
    [
        {
            "idx":0,
            "path":"/hello.bin"
        },
        {
            "idx":1,
            "path":"/blinky.bin"
        }
    ]
}

```

```

    }
}
}

```

It means there are two image files: *hello.bin* and *blinky.bin*, with their own index number. More image files can be added into the list if needed.

To integrate the cJSON into the bootloader project, add the *cJSON.h* and *cJSON.c* files, as shown in [Figure 5](#).

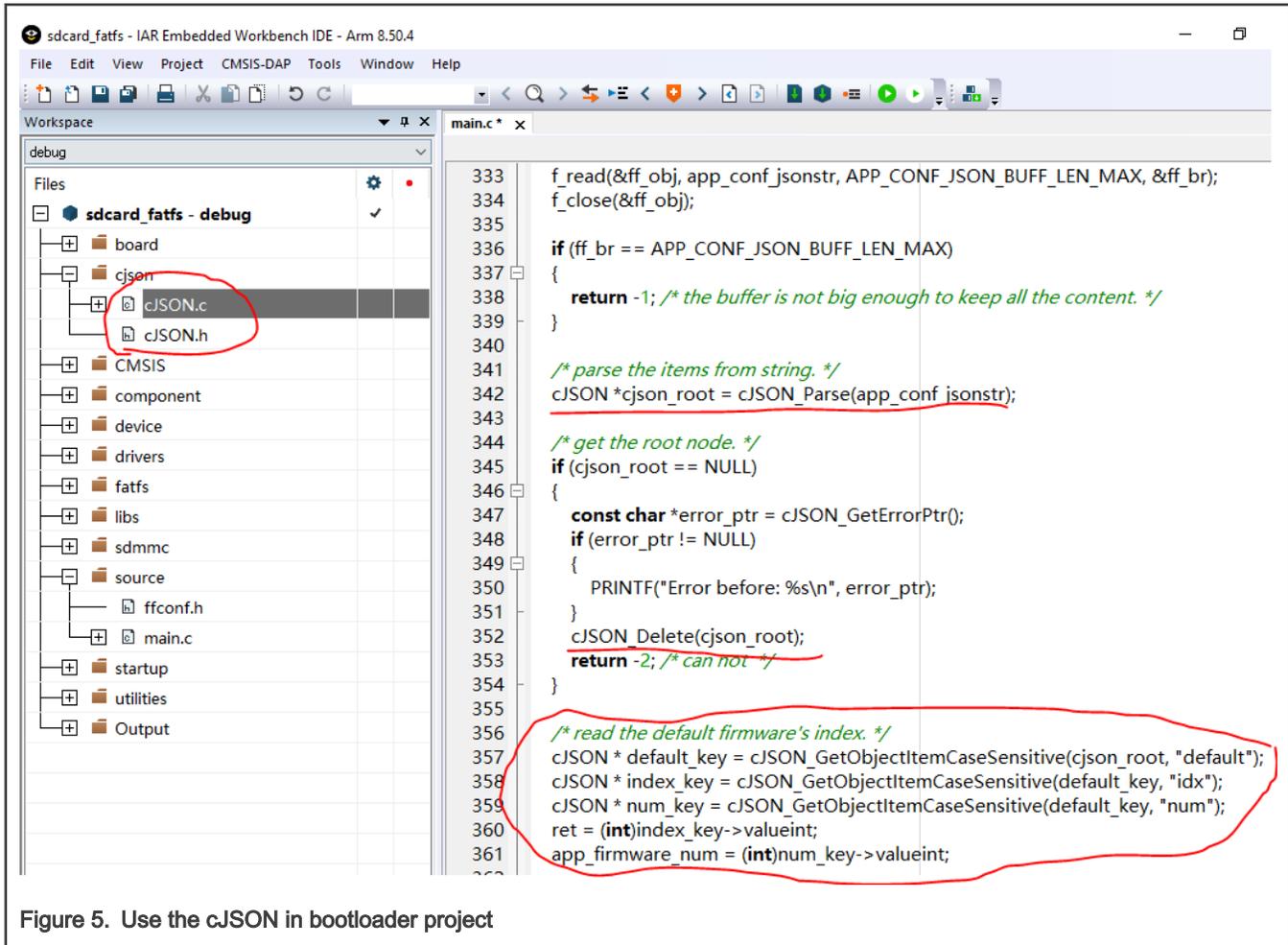


Figure 5. Use the cJSON in bootloader project

For the detailed usage about cJSON, see the *readme.md* file in the repository.

For the detailed coding work about the whole application demo project, see AN13113SW.

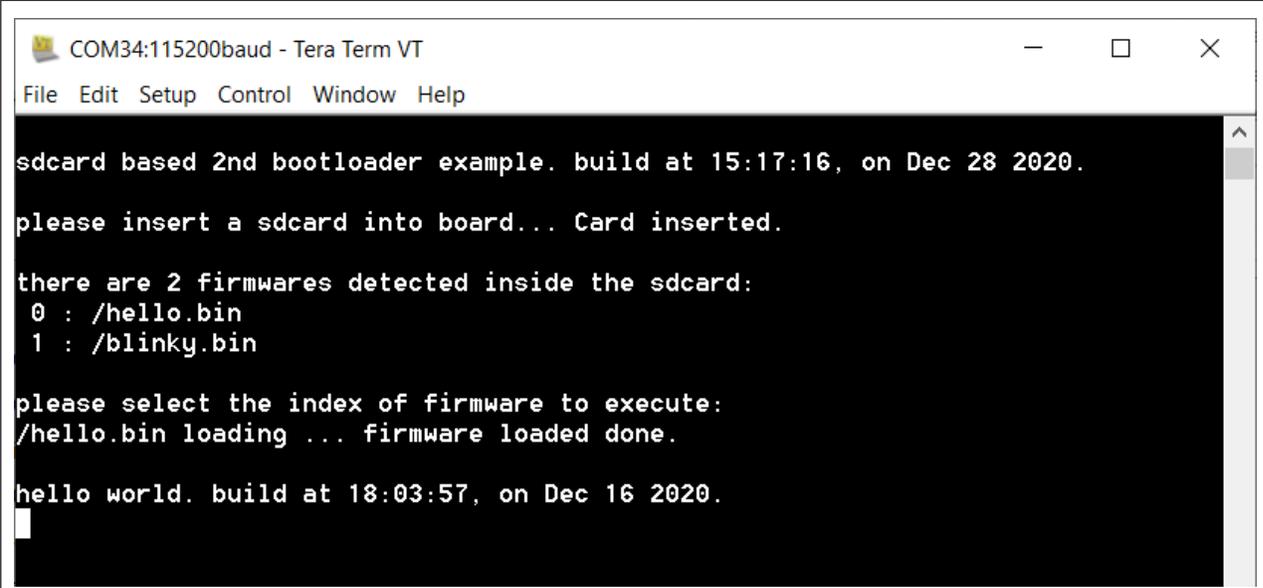
4 Run demo project

After the POR, the bootloader software in the chip's internal flash runs first. It reads the SD card to detect the available firmware image files and tells available options to users through the terminal, based on the UART. Users make the selection. Then the bootloader software loads the selected image files from SD card to internal memory of the chip, SRAM, and execute.

To run the demo project, please follow the steps:

1. Build the *app_hello* and *app_blinky* projects to create the *hello.bin* and *blinky.bin* files. Actually, there are also the pre-created ones in the attachment.
2. Plug in the SD card to PC, copy the *hello.bin*, *blinky.bin* and the *conf.json* files into the root directory of file system on SD card, and then unplug the SD card from PC. Now, the SD card is ready.

3. Build the `bootloader_sdcard_fatfs` project and download the image into LPC54608 EVK board.
4. Plug in the SD card to the LPC54608 EVK board and reset the board. Now the demo starts.
5. Watch the terminal and make the interaction with the board. The log is as seen in [Figure 6](#).



```
COM34:115200baud - Tera Term VT
File Edit Setup Control Window Help
sdcard based 2nd bootloader example. build at 15:17:16, on Dec 28 2020.
please insert a sdcard into board... Card inserted.

there are 2 firmwares detected inside the sdcard:
0 : /hello.bin
1 : /blinky.bin

please select the index of firmware to execute:
/hello.bin loading ... firmware loaded done.

hello world. build at 18:03:57, on Dec 16 2020.
```

Figure 6. Terminal interaction with demo board

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© NXP B.V. 2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: January 20, 2021

Document identifier: AN13113

